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Each chapter is a combination of theory followed by review exercises to be completed as traditional homework assignments. Full solutions to all of the review exercises are available in the last appendix. Procedures for labs then follow that allow the student to implement the concepts in a hands on manner. The materials required for the labs

Introduction to Digital Logic with Laboratory Exercises

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synthesizing the Verilog designs.. The Three Basic Gates.  
NOT gate inverts the logic state of input, so if x is 0, then y is 1 or if x is 1 then y is 0.

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